

*Fig. 1*

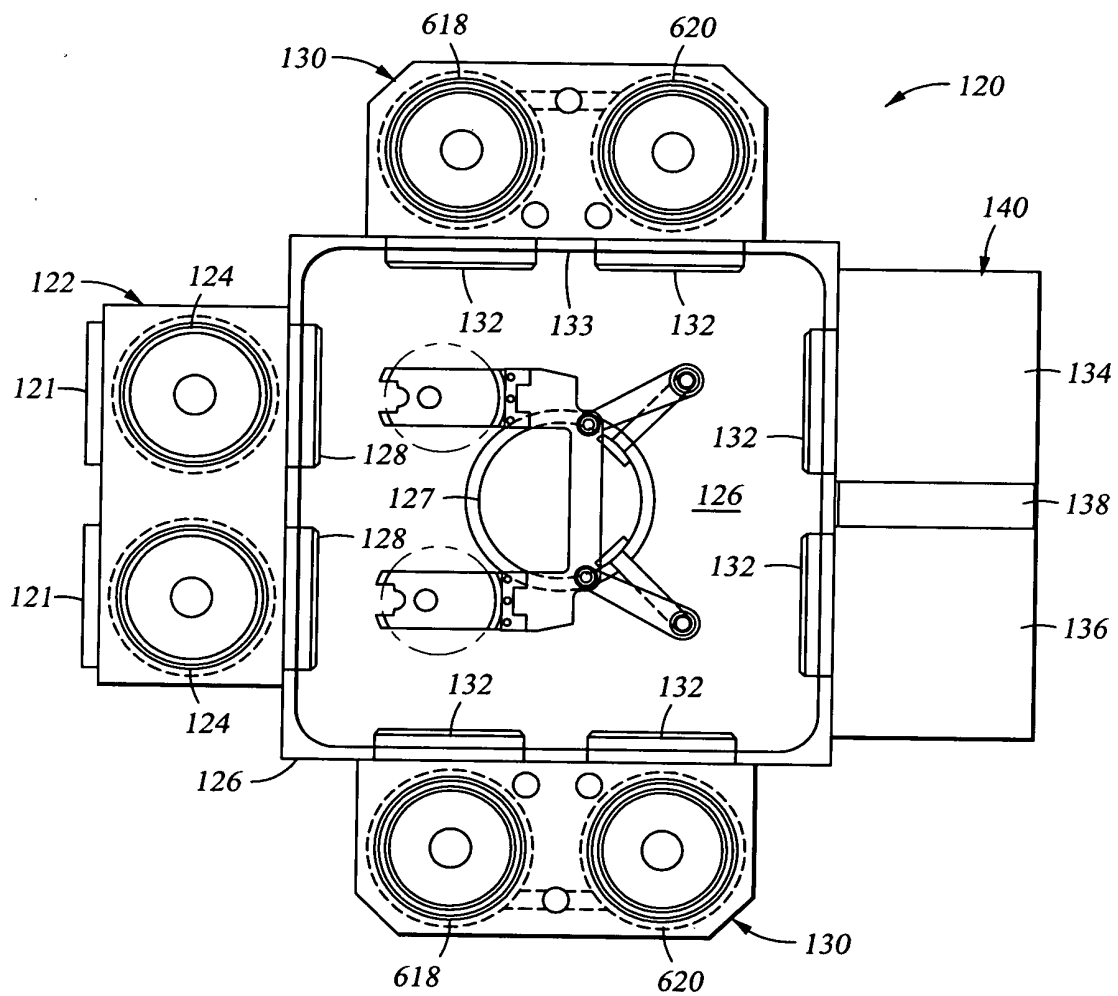
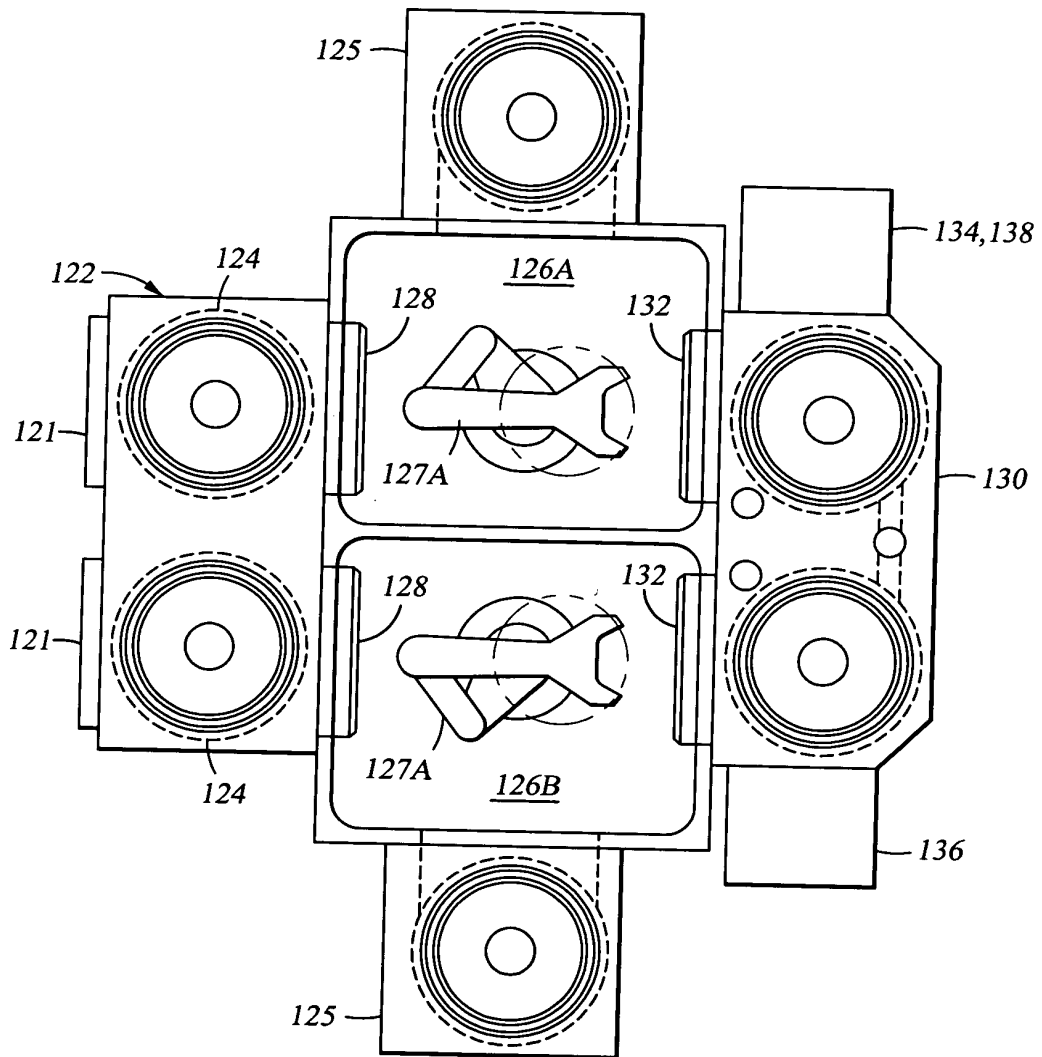


Fig. 2A

*Fig. 2B*

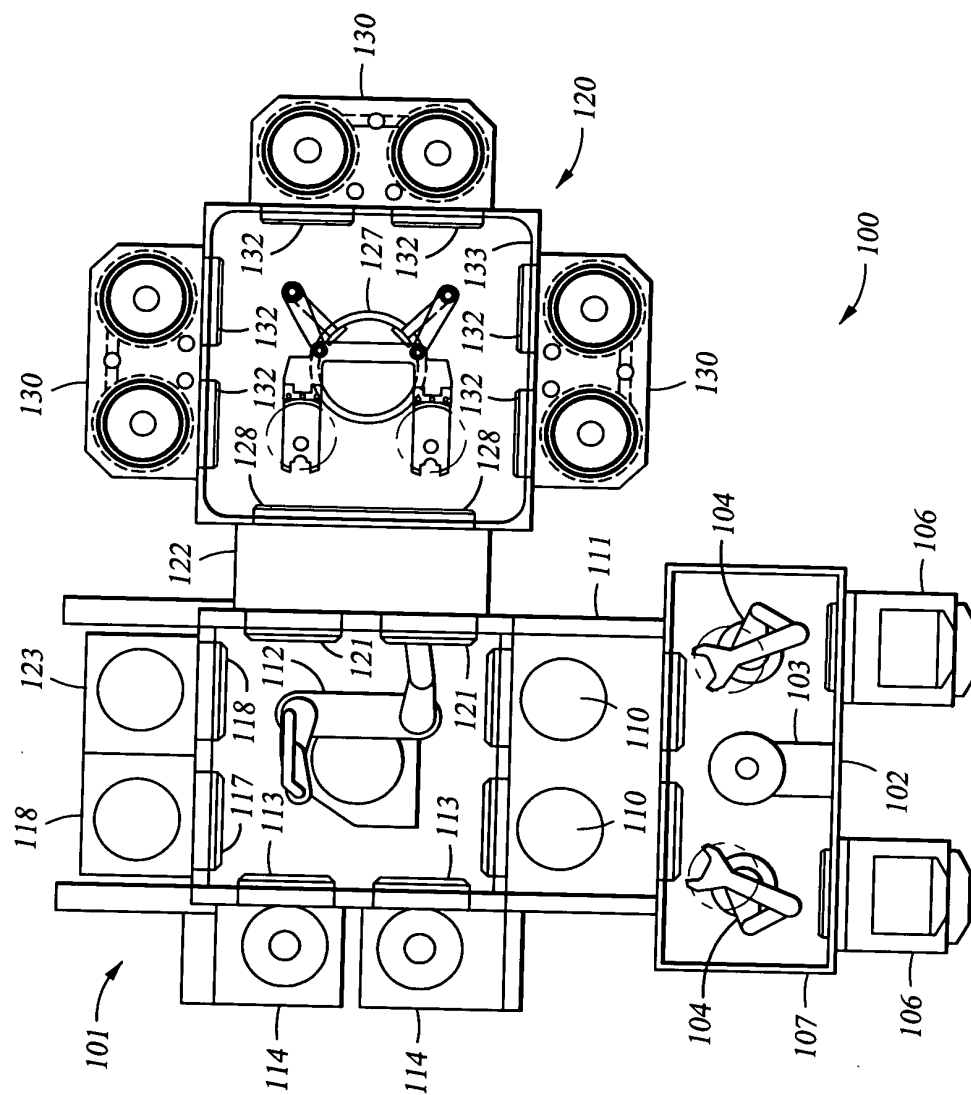


Fig. 3A

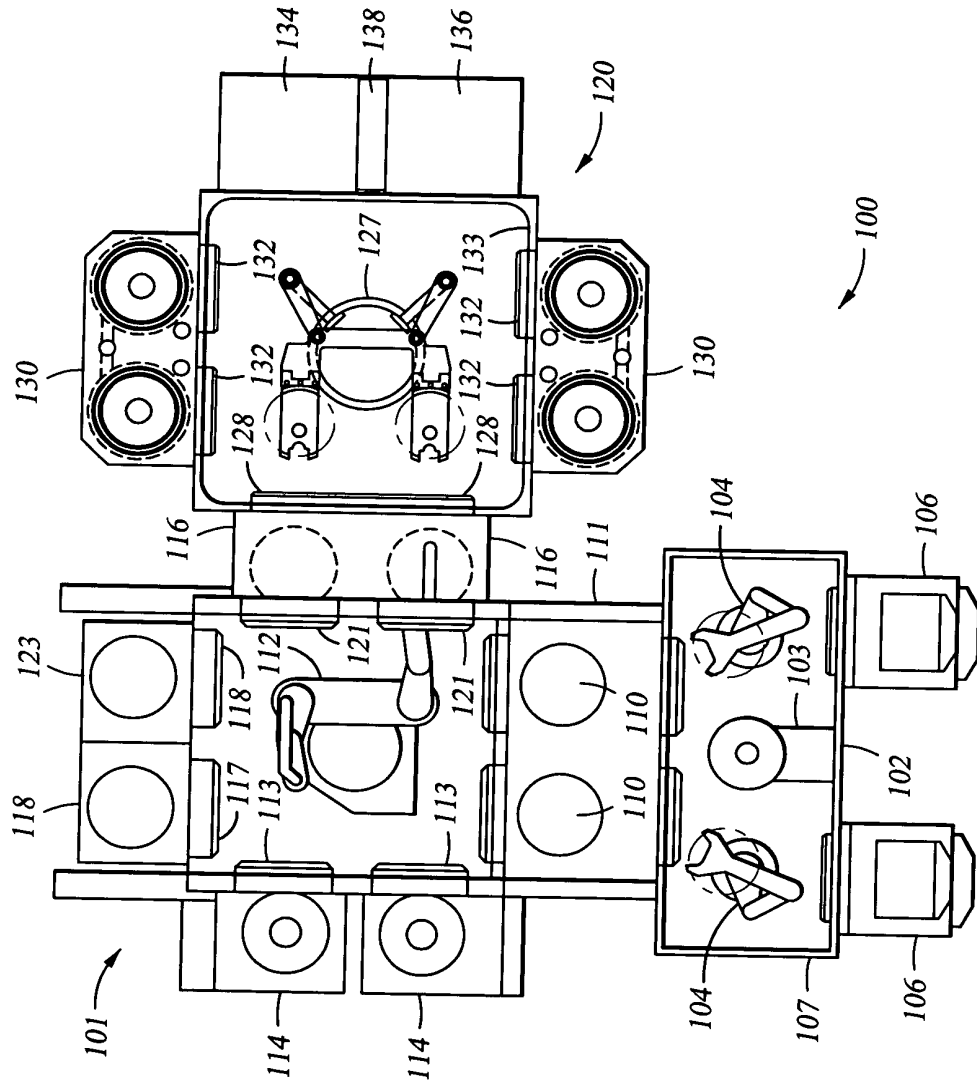


Fig. 3B

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6/17

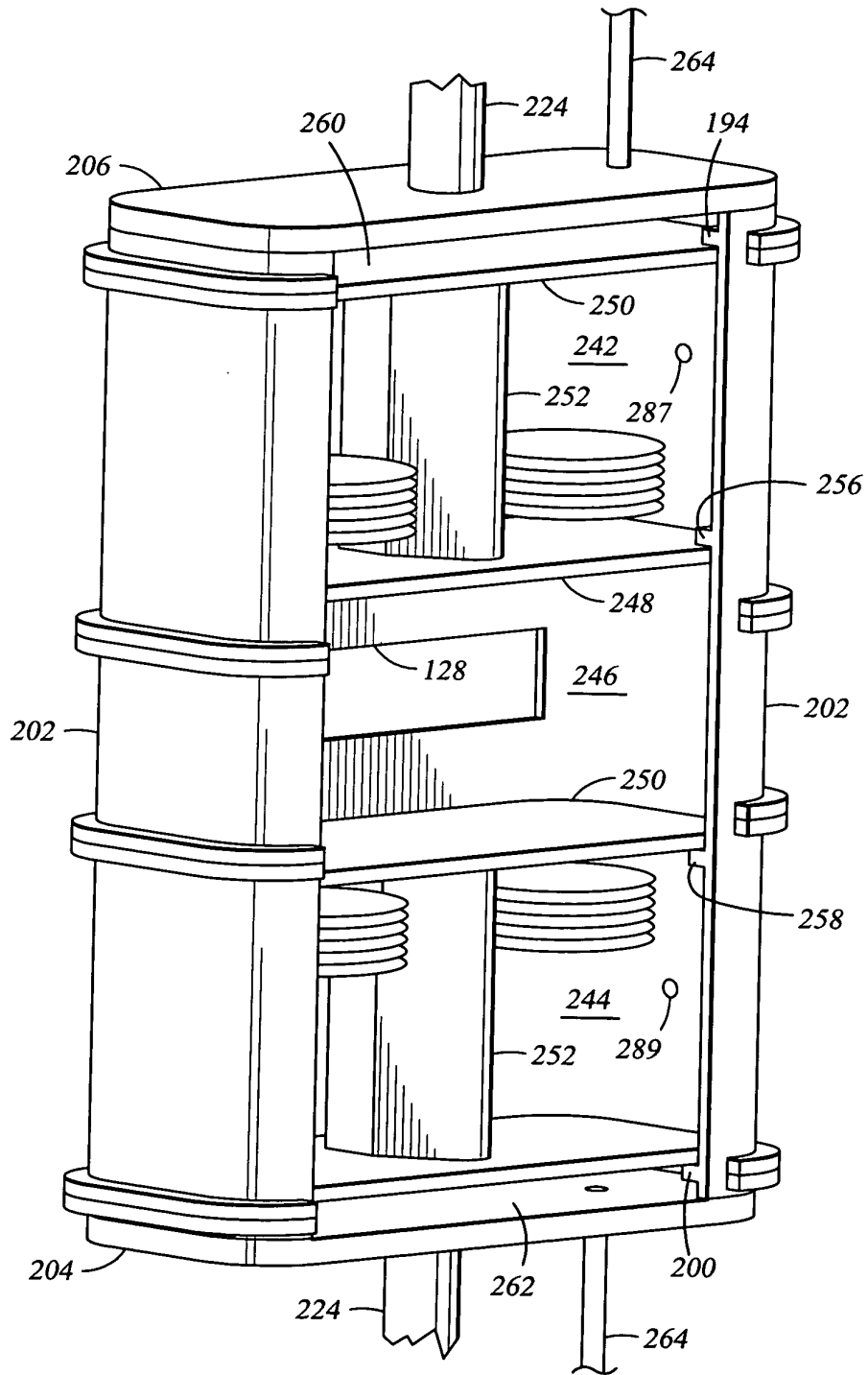
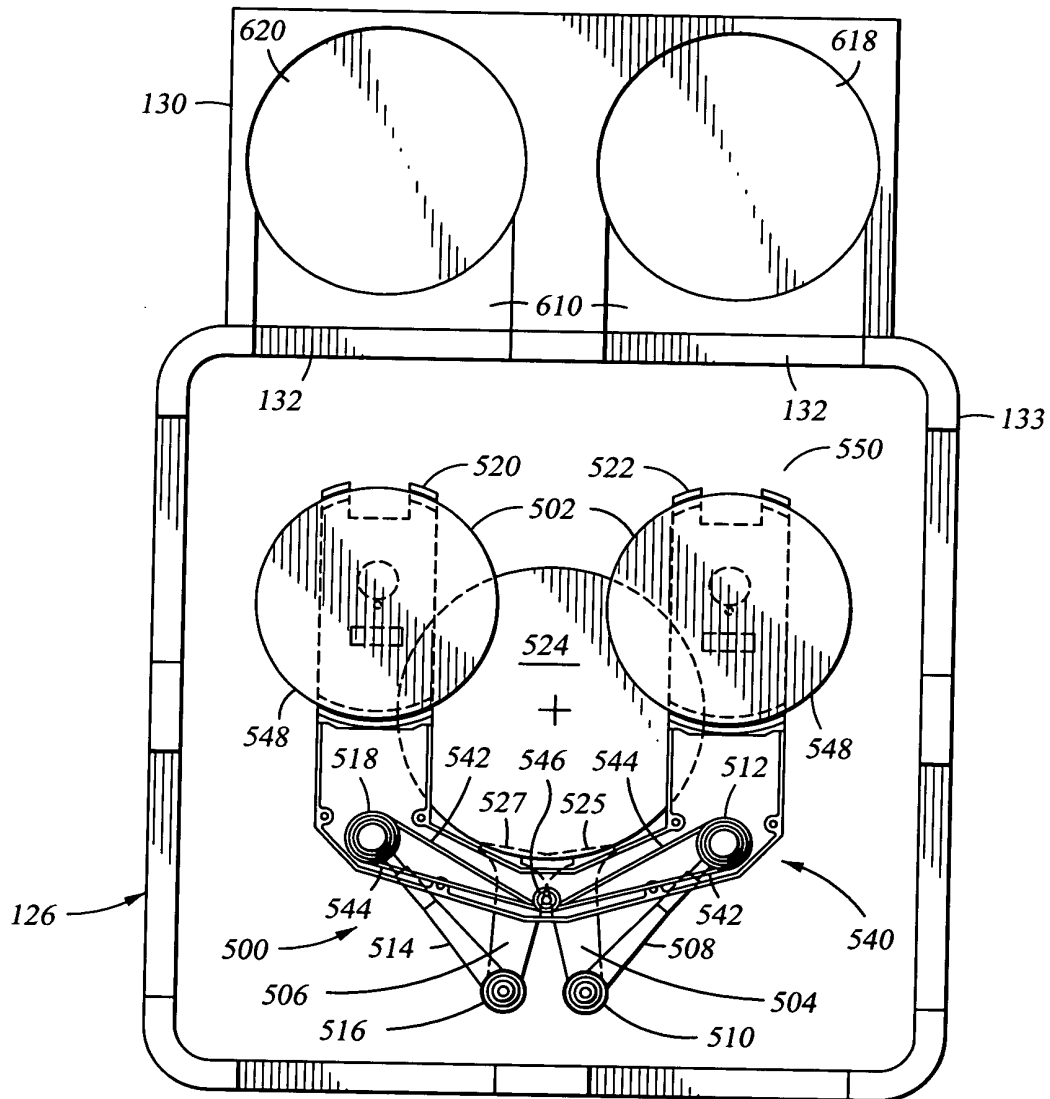


Fig. 4

*Fig. 5*

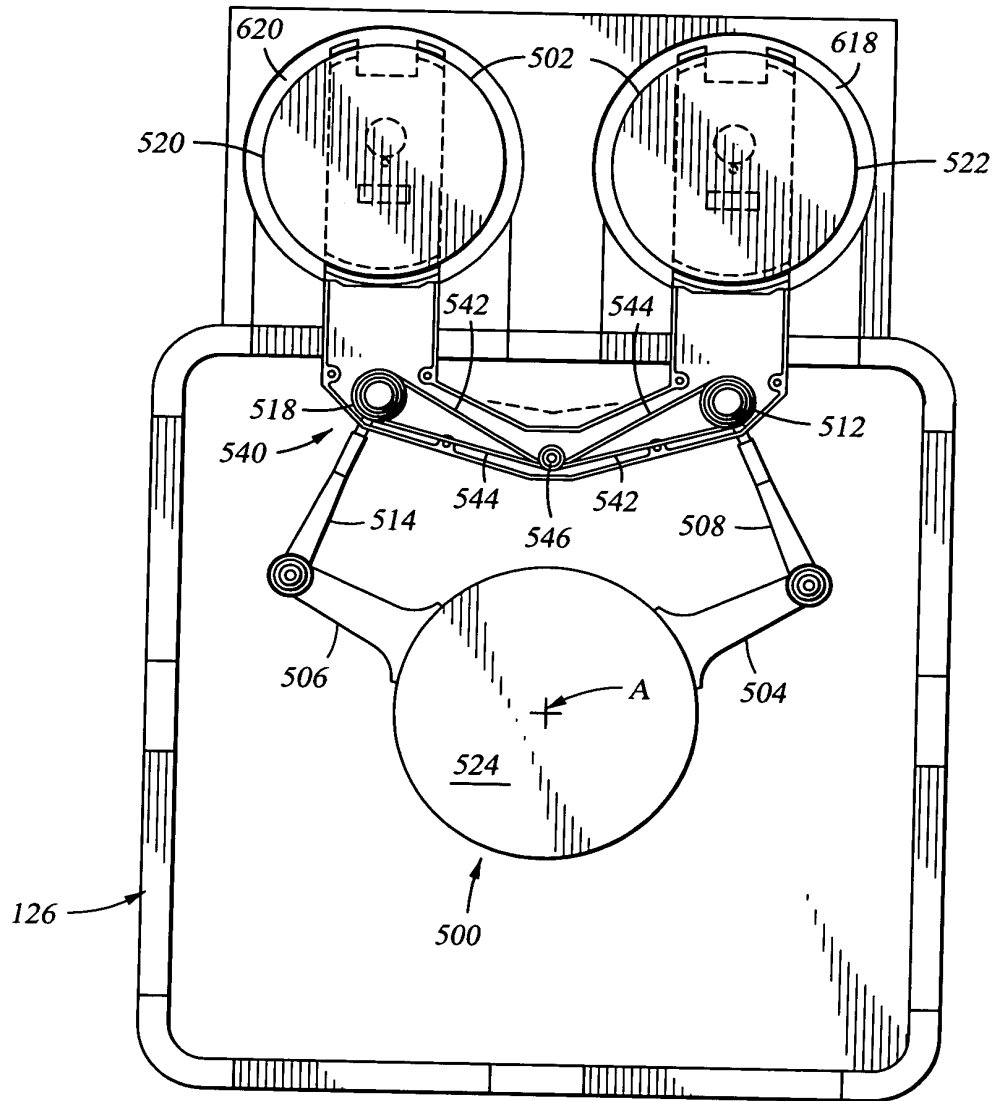


Fig. 6



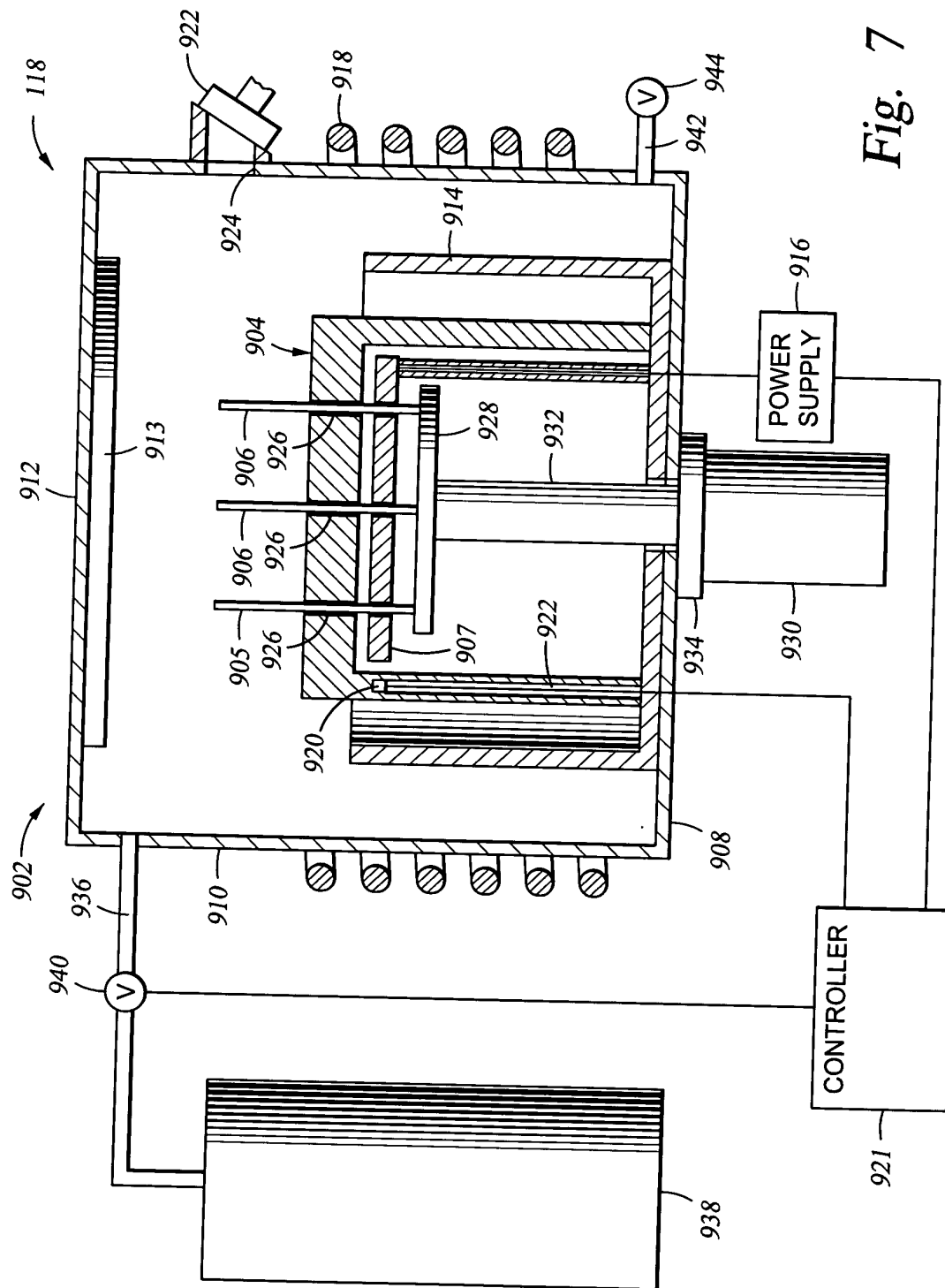
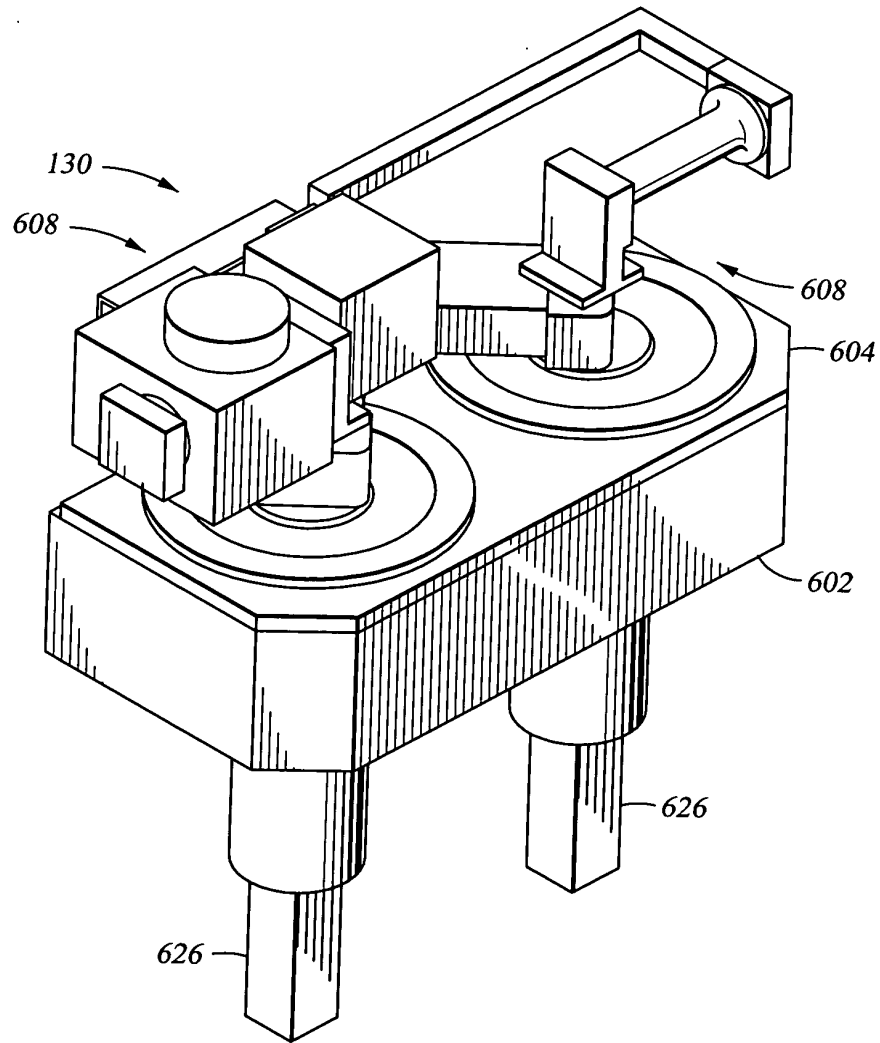
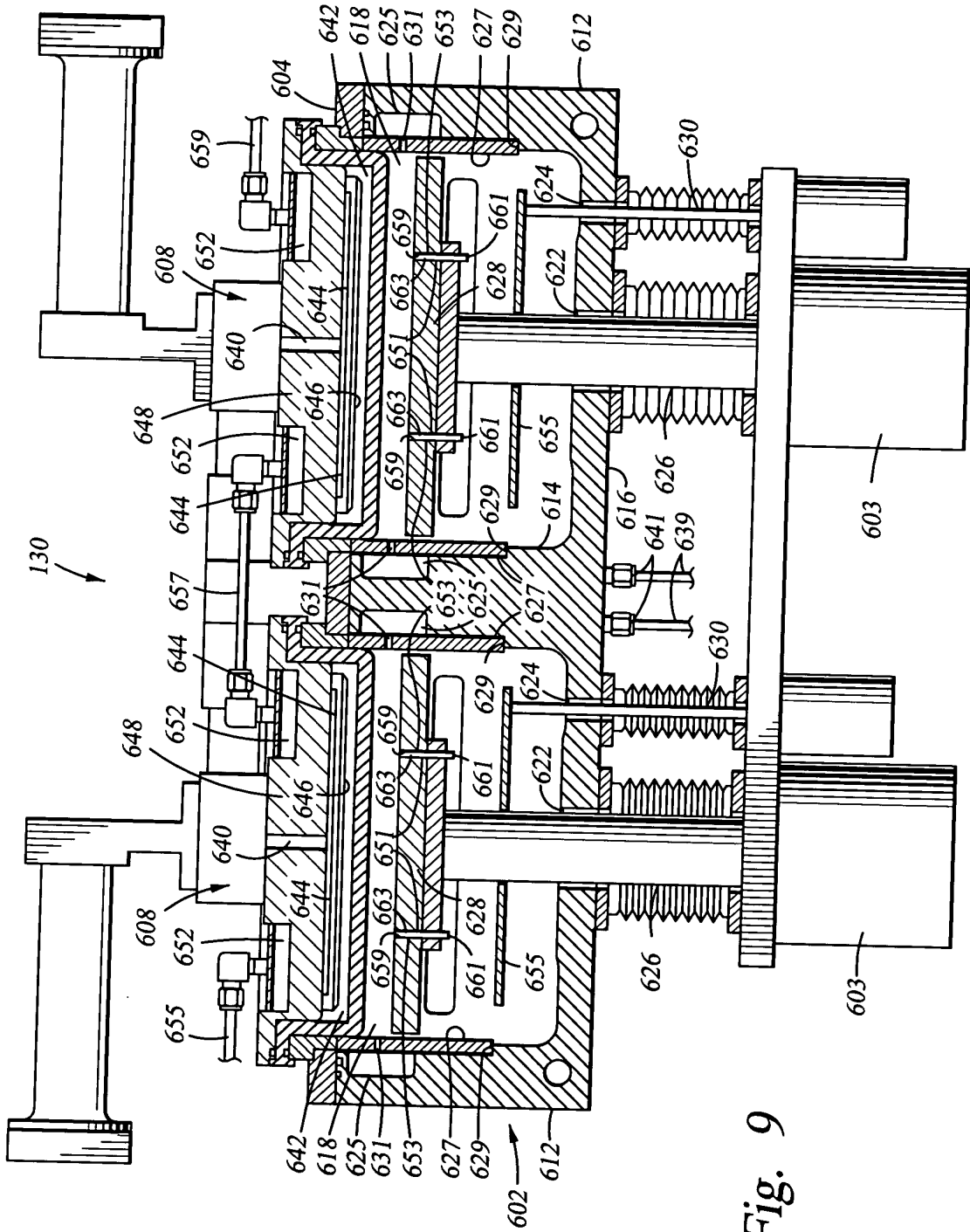


Fig. 7

*Fig. 8*

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12/17

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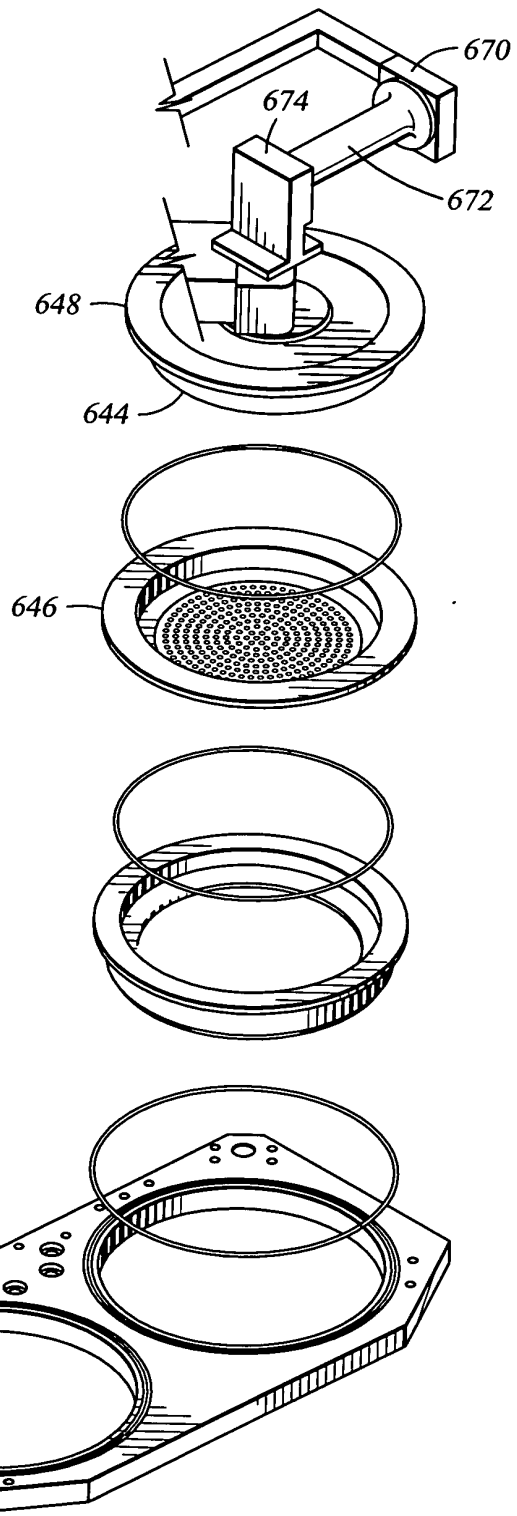


Fig. 10

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13/17

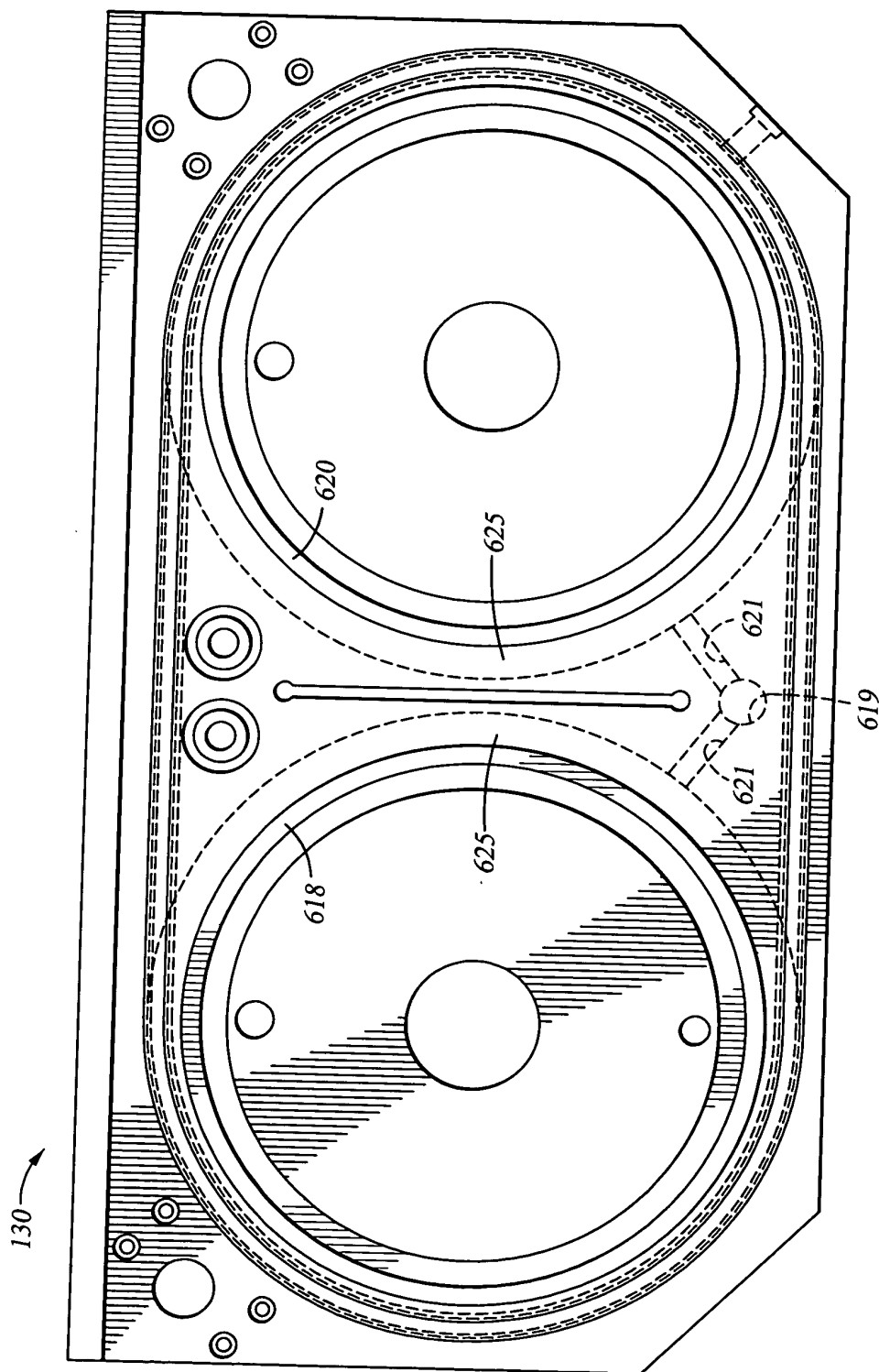
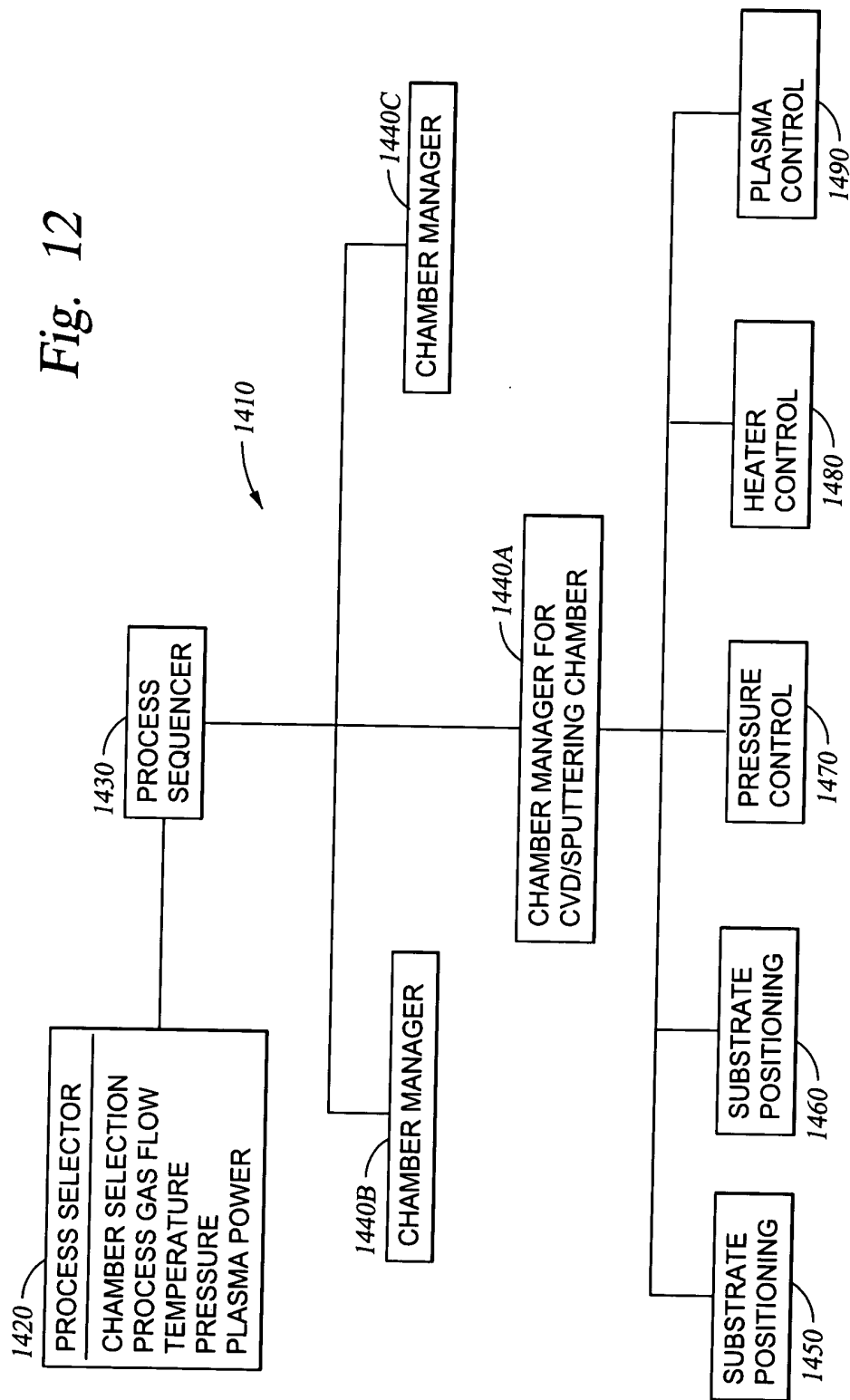


Fig. 11

Fig. 12



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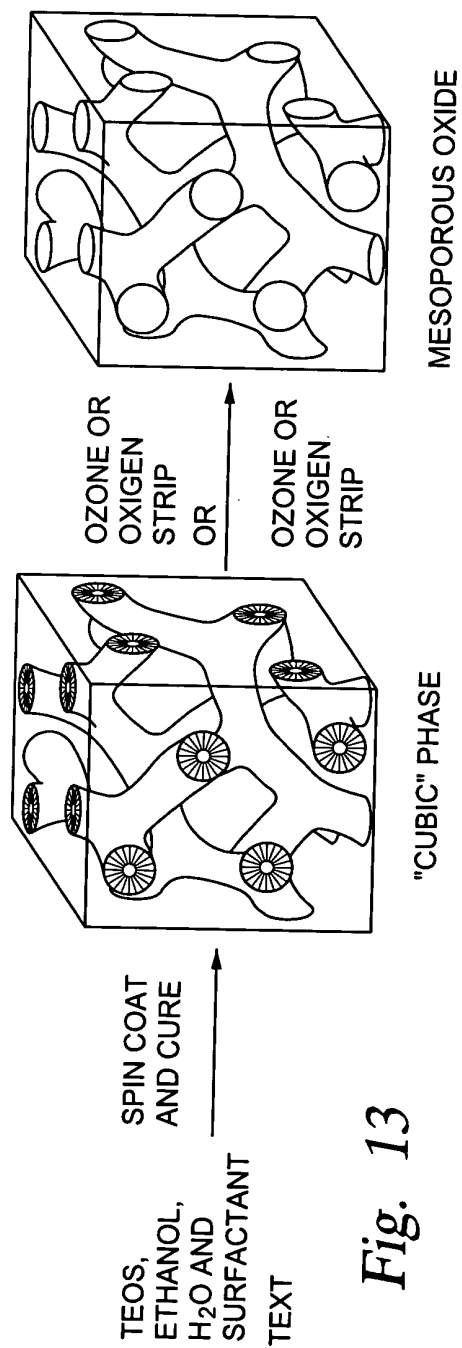


Fig. 13

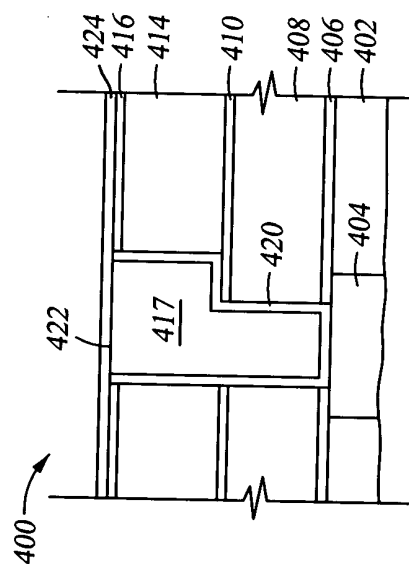


Fig. 14

Fig. 15A

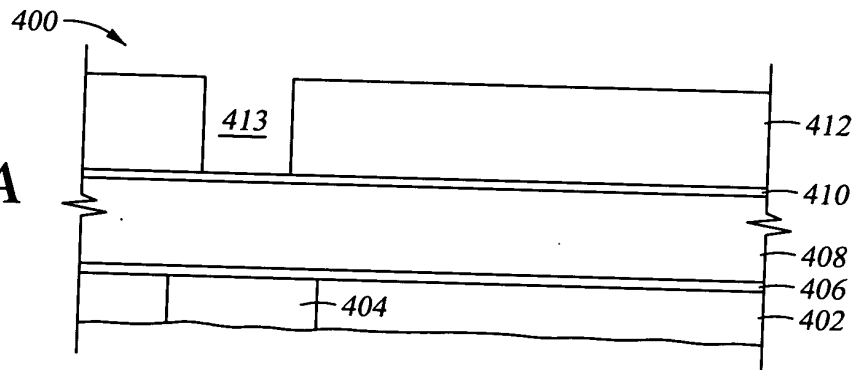


Fig. 15B

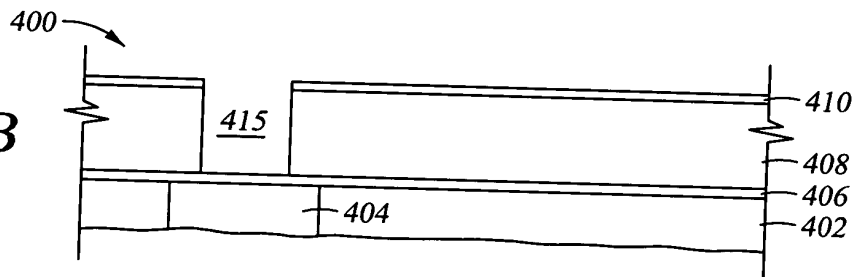


Fig. 15C

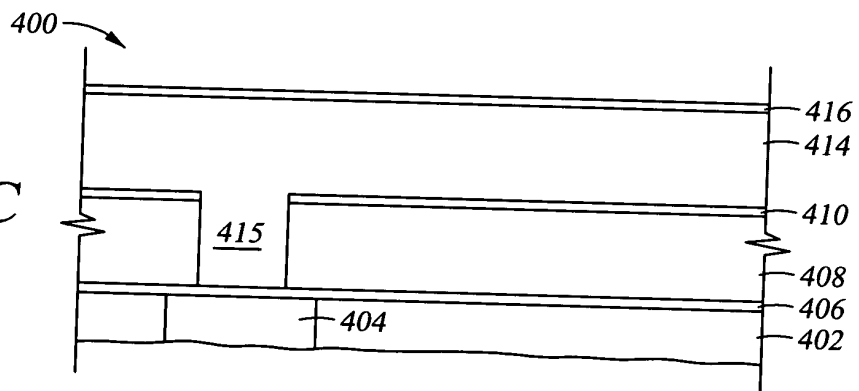
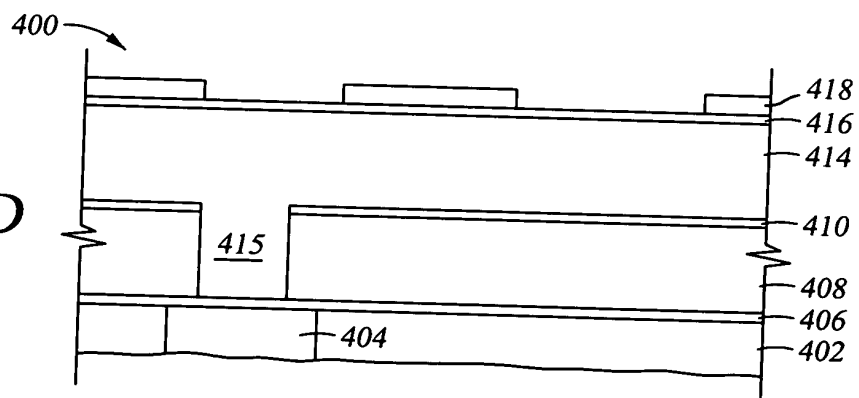


Fig. 15D



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[illegible]

A cross-sectional view of a semiconductor device. A substrate 402 is shown at the bottom. A gate structure 404 is formed on the substrate. A trench 410 is formed in the gate structure. The trench has a bottom surface 406 and side surfaces 408. A layer 414 is formed on the side surfaces 408 of the trench. A layer 416 is formed on the bottom surface 406 of the trench. A layer 417 is formed on the top surface of the gate structure 404. An arrow 400 points to the top surface of the gate structure 404.

A cross-sectional view of a multi-layered structure 400. The structure consists of several layers and components. At the top is a thin layer 422. Below this is a layer containing rectangular blocks 417 and 420, separated by a vertical line 416. Below this layer is another layer 410, which contains a large rectangular block 420. At the bottom is a layer 402, which contains a rectangular block 404. The entire structure is bounded by a top layer 408 and a bottom layer 406. A vertical line 414 is shown on the right side of the structure. A wavy line 400 is shown on the left side of the structure.

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